PCB Layout-Based Spatiotemporal Graph Convolution Network for Anomaly Prediction in Solder Paste Printing

Binkun Liu, Yu Kang, *Senior Member, IEEE*, Yun-Bo Zhao, *Senior Member, IEEE*, Yang Cao, *Member, IEEE*, and Zhenyi Xu

***Abstract*— Predicting solder paste printing anomaly on the printed circuit board (PCB) can improve first-pass yield and reduce rework costs. Considering the impact of the PCB layout on the quality of solder paste printing, we propose a PCB layout-based spatiotemporal graph convolution network, in which we construct a graph to model the spatial distribution of solder pads. Specifically, since the printing quality is related to the spatial distribution of the pads, we convert the PCB to a graph according to the Pearson correlation of the printing quality and then trim the edges of the graph with a correlation threshold to model the spatial distribution of solder pads. To model the time-varying physicochemical properties of the solder paste, normalize the production time, calculate the attention of the production time, and reconstruct the printing quality based on the attention. Then, we devise a weighted loss to improve the performance of predicted printing of defective products due to the scarcity of defective products. Ultimately, the predicted printing quality is compared with the inspection threshold to estimate the degree of anomaly. The proposed method is validated on six days of real solder paste printing data, improving the average $F1$ score by 0.057 and the average accuracy by 0.022 for three typical anomalous printing behaviors over two temporal prediction scales.**

***Index Terms*— Solder paste printing, surface mount technology, temporal anomaly prediction.**

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Binkun Liu is with the Department of Automation, University of Science and Technology of China, Hefei 230026, China, and also with Anhui Engineering Research Center for Intelligent Applications and Security of Industrial Internet, Anhui University of Technology, Ma'anshan, Anhui 243032, China (e-mail: liubink@mail.ustc.edu.cn).

Yu Kang is with the Department of Automation, University of Science and Technology of China, Hefei 230026, China, also with the Institute of Artificial Intelligence, Hefei Comprehensive National Science Center, Hefei 230088, China, and also with the Key Laboratory of Technology in GeoSpatial Information Processing and Application System, Chinese Academy of Sciences, Beijing 100192, China (e-mail: kangduyu@ustc.edu.cn).

Yun-Bo Zhao and Yang Cao are with the Department of Automation, University of Science and Technology of China, Hefei 230026, China, and also with the Institute of Artificial Intelligence, Hefei Comprehensive National Science Center, Hefei 230088, China (e-mail: ybzhao@ustc.edu.cn; forrest@ustc.edu.cn).

Zhenyi Xu is with the Institute of Artificial Intelligence, Hefei Comprehensive National Science Center, Hefei 230088, China (e-mail: xuzhenyi@mail.ustc.edu.cn).

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I. Introduction

THE solder paste printing process is an essential step in the assembly of the printed circuit board (PCB) [1], [2], [3]. This process establishes a permanent electrical and mechanical connection between the component and the PCB [4], [5]. Solder paste printing anomaly is that the PCB does not meet production standards during the solder paste printing process. It has a significant impact on production efficiency and costs [6], [7]. For a typical laptop manufacturer, solder paste printing abnormalities account for basically 10% of the total number of PCBs in the solder paste inspection. Approximately 50–70% of PCB defects are related to the solder paste printing step, even passing the solder paste inspection [8], [9], [10].

To avoid solder paste printing anomaly, for economic and time-sensitive reasons, the natural idea is to predict the anomaly during production and adjust the solder paste printing parameters according to the extent of the anomaly [11], [12], [13], thus regulating the printing quality [14]. A good abnormality prediction can sense solder paste printing abnormality and the degree of abnormality in advance, preparing for the subsequent adjustment of solder paste printing parameters. This enables the advanced elimination of solder paste printing anomalies. Therefore, as an important prerequisite for avoiding solder paste printing anomaly, predicting solder paste printing anomaly is a core issue.

The implementation of solder paste printing anomaly prediction during production mainly utilizes the multivariate time-series anomaly prediction technique. The existing multivariate time-series anomaly prediction methods [15], [16], [17] mainly utilize the correlation among the variables and the temporal characteristics of the variables for prediction, without the need to predict the degree of anomaly. However, in solder paste printing anomaly prediction, merely predicting whether an anomaly will occur or not is not enough for subsequent adjustment of the solder paste printing machine parameters. Therefore, existing multivariate time-series anomaly prediction methods are difficult to apply directly.

Current solder paste printing anomaly prediction methods typically predict printing quality and then compare it to production standards. There are two different typical application scenarios. A typical scenario [18], [19] is that factories aim to efficiently determine whether the set process parameters will cause printing quality abnormality before production

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begins. Methods such as Taguchi methods [20] and multilayer perceptrons [21] are used to model the nonlinear relationships between process parameters and printing quality. Another typical scenario [22], [23], [24], [25], [26] that we are concerned about is that factories want to predict printing quality anomalies after production starts, to dynamically adjust process parameters and avoid producing defective products. In this case, time-series regression models such as SVR [23] and LSTM [26] are used to analyze the temporal patterns of solder paste printing quality, utilizing the temporal closeness of solder paste printing to predict whether quality anomaly will occur in the future. Alelaumi et al. [22] proposed a new multitemporal intelligent anomaly prediction framework to improve the first pass rate and reduce the rework cost on PCB assembly lines. In the first phase, an exponentially weighted moving average control chart based on the random forest is designed to monitor the highly autocorrelated solder paste printing process. In the second stage, statistical features are designed based on quality-series data to predict solder paste printing anomaly in advance through adaptive boosting techniques. Wang et al. [26] introduced more powerful deep learning algorithms rather than previous machine learning algorithms. They used a combination of wavelet transforms and LSTM to analyze real-time and historical printing performance to predict future printing performance. Wang et al. [23] attempted to predict the quality of solder paste printing while adjusting the parameters of the solder paste printing machine. The SVR model is utilized to predict the future solder paste volume based on the real-time solder paste volume and then the PSO algorithm is utilized to adjust the solder paste printing parameters based on the predicted volume. Thielen et al. [24] developed an automated machine learning method to reduce model development time. This approach leverages process data and historical quality information to predict solder quality, specifically in terms of height, area, and volume. Seidel et al. [25] introduced a scalable machine learning-enabled framework for quality prediction in solder paste printing. This framework parses details of the entire production process and rapidly analyzes correlations between inputs and printing quality.

However, the temporal pattern-based approaches tend to focus on the apparent temporal closeness rather than the latent spatial correlation. This may result in printing quality not constrained by irregular PCB layouts, thus reducing predictive performance. Spatial correlation is caused by neighborhood similarity and local structure dependence. Neighborhood similarity means that the variations in solder paste printing quality of adjacent pads are highly correlated. Local structure dependence means that similar pad layouts lead to higher correlations, due to component pitch as one of the factors influencing solder paste printing quality.

To model the effect of PCB layout on the variation of solder paste printing quality, we propose a PCB layout-based spatiotemporal graph convolution network, in which we construct a graph to model the spatial distribution of solder pads. Specifically, given that the solder paste printing quality is correlated with the spatial distribution of pads on the PCB, we construct a weighted graph that implies the spatial structure

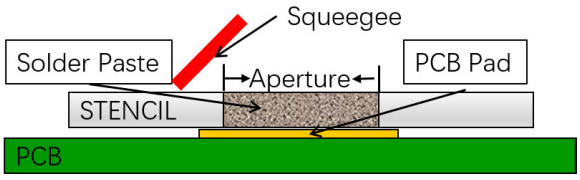

Fig. 1. Process of solder paste printing.

by the Pearson correlation between the solder paste printing qualities and then trim the edges of the graph by the correlation threshold. Considering that the physicochemical properties of the solder paste are time-varying [27], [28], [29], we attempt to encode the effect of time on printing quality and normalize time and then calculate the attention to time and reconstruct the solder paste printing quality characteristics based on the attention. Due to the scarcity of defective products in solder paste printing, we devise a weighted loss to increase the weight of defective products and promote the model to focus on printing quality anomaly. Ultimately, the predicted printing quality is compared with the inspection threshold to estimate the degree of anomaly.

All in all, the main contributions of the proposed method are summarized as follows.

1) For the solder paste printing anomaly prediction problem, this is the first time to analyze the significant impact of irregular PCB layout on the solder paste printing quality variation, strongly facilitating the understanding of the problem.
2) To the best of our knowledge, this is the first work to use graph modeling of the irregular PCB layout to predict solder paste printing anomaly and is evaluated on a six-day real solder paste inspection dataset. The average $F1$ score improves by 0.057 and the average accuracy improves by 0.022 for three typical printing behavior anomalies over two time prediction scales.

II. Overview

A. Solder Paste Printing Process

Fig. 1 illustrates the solder paste printing process. The squeegee covers the solder paste on the stencil, the mesh on the stencil and the PCB pad correspond one by one, and the solder paste through the mesh penetrates the pad. The following is a breakdown of the solder paste printing process.

1) *First is Stencil Preparation:* A stencil is a thin sheet of metal or polymer with openings or apertures that correspond to specific locations on the PCB pads.
2) *Then Comes the Alignment of the Stencil:* Align and secure the stencil to the PCB, ensuring that the apertures are precisely aligned with the pads on the PCB. Next, apply the solder paste to the stencil. According to the printing parameters, solder paste is applied to one end of the stencil and then pushed through the aperture by a squeegee, depositing a controlled amount of paste onto the PCB pads.
3) *The Last is the Solder Paste Inspection:* After applying the solder paste, the stencil is carefully removed from

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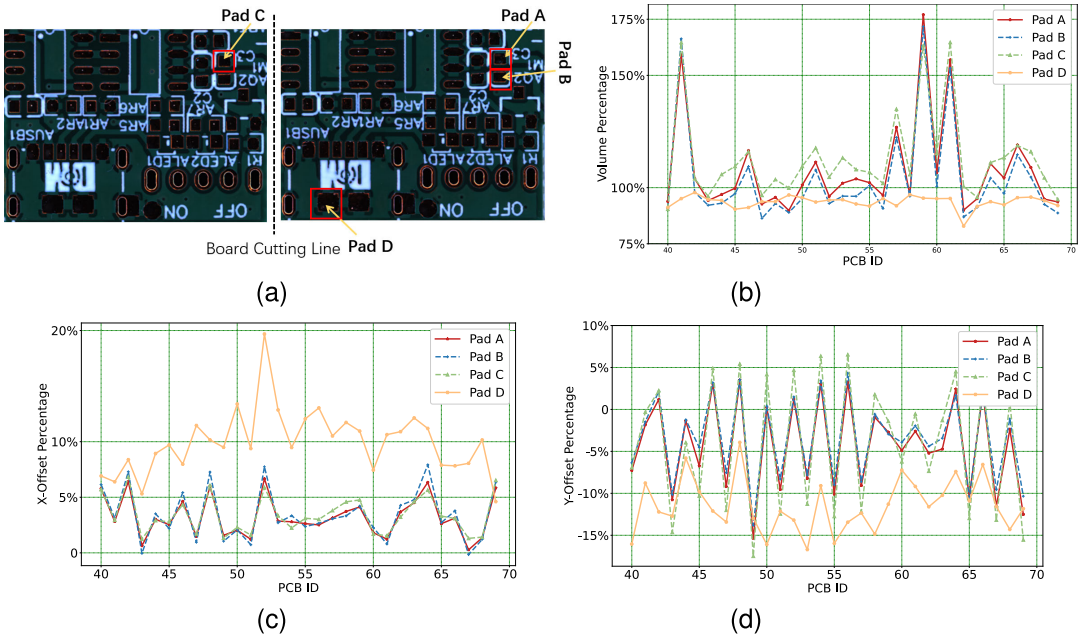

Fig. 2. Curves of solder paste volume, X-direction offset, and Y-direction offset for four pads. Pads A and B are adjacent to each other. Pads C and A share identical local structures. Pad D is further away from Pad A. (a) Pad distribution. (b) Solder paste volume curves for four pads. (c) Solder paste X-direction offset curves for four pads. (d) Solder paste Y-direction offset curves for four pads.

the PCB. The PCB is then inspected for misalignment of solder paste, insufficient or excessive solder paste, or any defects in the printing process.

B. Influence of the PCB Layout on Solder Paste Printing Quality

The positions of the pads are shown in Fig. 2(a). It can be observed that Pad A is adjacent to Pad B, while Pad D is located far away from Pad A. Pad C shares the same local structure as Pad A. This is due to manufacturers often employing a PCB panelization strategy, which involves printing multiple identical PCBs simultaneously and then cutting them along predetermined board cutting lines. The board cutting line is depicted by the black dotted line in Fig. 2(a). Due to size and resolution constraints, only two partial images on either side of the board cutting line are shown here. It should be noted that the board cutting line is included for illustrative purposes only.

The influence of the PCB layout on solder paste printing quality reflects the effects of neighborhood similarity and local structure dependence. Specifically, Fig. 2(b)–(d) shows the curves of solder paste printing volume, X-direction offset, and Y-direction offset for four pads, respectively. It can be seen that Pads A, B, and C exhibit similar trends in terms of three solder paste printing quality attributes, while Pad D shows some differences. This is because Pads A and B are neighboring and the printing quality variation follows the principle of local similarity. Pads A and C exhibit identical local structures. Component pitch is a critical factor influencing solder paste printing quality. Therefore, despite their distance, and even if they are not located on the same PCB, they exhibit similar printing quality. Pad D shows some differences due to its distance from Pad A, as well as local structural inconsistencies.

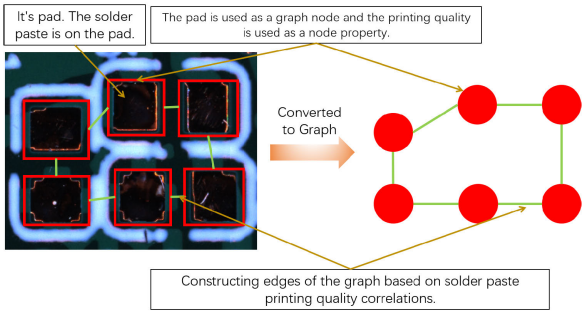

Fig. 3. Schematic of converting a PCB to a graph.

C. Definition

Definition 1 (PCB Layout Graph): As shown in Fig. 3, the black areas in the red boxes are the pads, and in the solder paste printing process, the solder paste will be printed to the location of the pads. At time t, the PCB layout graph $G_t = (V_t, A)$ has the pads in the red boxes of Fig. 3 as nodes, and the green lines indicating the correlations of printing qualities as edges. $V_t = [x_t^1, \ldots, x_t^M] \in \mathbb{R}^M$, V_t is the node of the graph, M denotes the number of pads, and $x_t^i \in \mathbb{R}$, $i = 1, \ldots, M$, x_t^i denotes the quality inspection feature of the ith pad at moment t. A is the adjacency matrix obtained by edge aggregation.

D. Problem Setting

Our task is to predict primarily whether future PCB solder paste printing quality will be abnormal based on historical PCB solder paste printing quality data and then to predict the extent of the abnormality.

Given the graph representation of the PCB at the past N production moments $\mathcal{G}_{t_1,t_N} = [G_{t_1}, \ldots, G_{t_N}]$, the model $f(\cdot)$

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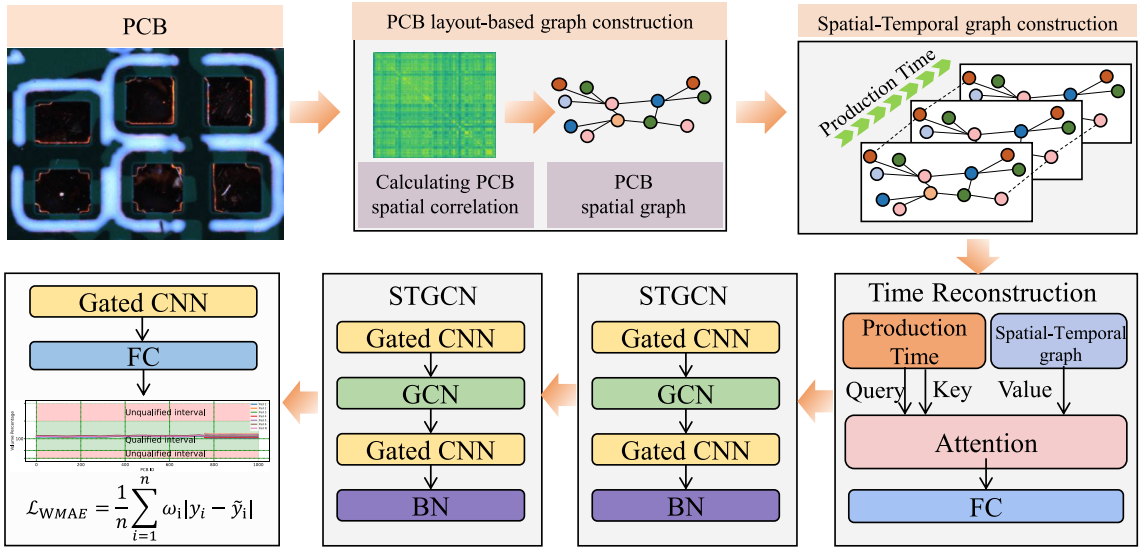

Fig. 4. Framework of the PCB layout-based spatiotemporal graph convolution network for solder paste printing anomaly prediction.

is built to predict the printing quality of each solder paste of the PCB at T future production moments, denoted as $\widetilde{\mathcal{G}}_{t_{N+1},\ t_{N+T}} = [\widetilde{G}_{t_{N+1}}, \ldots, \widetilde{G}_{t_{N+T}}]$. The formula is as follows:

$$\widetilde{\mathcal{G}}_{t_{N+1},t_{N+T}} = f\left(\mathcal{G}_{t_1,t_N}\right). \tag{1}$$

Then, the predicted results $\widetilde{\mathcal{G}}_{t_{N+1},\ t_{N+T}}$ are compared with the production standard to identify whether and to what extent an abnormality has occurred.

III. Method

A. Framework

Fig. 4 illustrates the framework of the PCB layout-based spatiotemporal graph convolution network. It consists of three main parts: PCB layout-based graph construction, temporal reconstruction, and spatiotemporal graph convolution. The PCB layout-based graph construction converts each PCB into a weighted graph through solder paste printing quality correlation to simulate the spatial structure of the PCB. Time reconstruction builds self-attention according to time to reconstruct PCB features to simulate the time-varying viscosity of the solder paste. The spatial–temporal graph convolutional network is employed to extract temporal closeness and spatial correlation features of solder paste printing quality. The proposed PCB layout-based spatiotemporal graph convolution network for solder paste printing anomaly prediction is described in detail in the following.

B. PCB Layout-Based Graph Construction

Initially, we chose the Pearson correlation coefficient to analyze the quality of solder paste printing. The formula is as follows:

$$c_{i,j} = \frac{\sum_{t=t_1}^{t_N}\left(x_t^i - \mu_{t_1,t_N}^i\right)\left(x_t^j - \mu_{t_1,t_N}^j\right)}{\sigma_{t_1,t_N}^i \sigma_{t_1,t_N}^j} \tag{2}$$

where $X_{t_1,t_N}^i = [x_{t_1}^i, x_{t_1+1}^i, \ldots, x_{t_N}^i] \in \mathbb{R}^{N\times 1}$ denotes the set of features of the ith solder paste from moment t_1 to moment t_N. μ_{t_1,t_N}^i is the mean of X_{t_1,t_N}^i and σ_{t_1,t_N}^i is the variance of X_{t_1,t_N}^i.

Then, we introduce a threshold function $T_\lambda(c)$ to prune the edges of the graph and remove the association between them when the correlation $c_{i,j}$ is less than λ. The threshold function $T_\lambda(c)$ is expressed as follows:

$$T_\lambda\left(c_{i,j}\right) = \begin{cases} c_{i,j}, & c_{i,j} \geq \lambda \text{ and } i \neq j \\ 0, & c_{i,j} < \lambda \text{ and } i \neq j \\ 0, & i = j. \end{cases} \tag{3}$$

From this, construct the adjacency matrix A

$$A = \begin{pmatrix} T_\lambda\left(c_{1,1}\right) & \cdots & T_\lambda\left(c_{1,M}\right) \\ \vdots & \ddots & \vdots \\ T_\lambda\left(c_{M,1}\right) & \cdots & T_\lambda\left(c_{M,M}\right) \end{pmatrix} \in \mathbb{R}^{M\times M}. \tag{4}$$

C. Time Reconstruction

Solder paste is one of the primary factors affecting printing quality, and its physical and chemical properties change gradually over time. Therefore, we need to consider the impact of time on printing quality. Let the real production time vector $\mathbf{t} = [t_1, t_2, \ldots, t_N] \in \mathbb{R}^{1\times N}$, first the vector $\mathbf{t}$ is normalized, and the formulation is as follows:

$$\dot{t}_i = \frac{t_i - t_1}{t_N - t_1}, \quad i = 1, \ldots, N. \tag{5}$$

The normalized production time vector $\dot{\mathbf{t}} = [\dot{t}_1, \dot{t}_2, \ldots, \dot{t}_N] \in \mathbb{R}^{1\times N}$ is obtained. To model the effect of production time on solder paste printing quality, temporal attention is calculated by production moments and the solder paste printing quality features are reconstructed in a weighted form derived from temporal attention.

Encoding the normalized production time vector $\dot{\mathbf{t}}$

$$e_k = W_1\dot{\mathbf{t}} + b_1 \in \mathbb{R}^{d\times N} \tag{6}$$

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$$e_q = W_1'\dot{\mathbf{t}} + b_1' \in \mathbb{R}^{d\times N} \tag{7}$$

where $W_1 \in \mathbb{R}^{d\times 1}$, $b_1 \in \mathbb{R}^d$, $W_1' \in \mathbb{R}^{d\times 1}$, $b_1' \in \mathbb{R}^d$ are trainable parameters, and d denotes the encoding dimension.

Calculate the temporal attention matrix Att of the production time with the following equation:

$$\text{Att} = \text{LeakyRelu}\big(e_k{}^T W_k^T\big)\text{LeakyRelu}\big(W_q e_q\big) \tag{8}$$

where $W_k \in \mathbb{R}^{d\times d}$ and $W_q \in \mathbb{R}^{d\times d}$ are trainable parameters.

Then, softmax is used to constrain Att to convert the attention score between solder pastes into a probability distribution between [0, 1] while highlighting the relationship between solder pastes

$$\text{Att}'_{i,j} = \frac{\exp\big(\text{Att}_{i,j}\big)}{\sum_{j=1}^{N}\exp\big(\text{Att}_{i,j}\big)}. \tag{9}$$

Lastly, the attention matrix Att′ obtained is used to reconstruct the feature $X^i_{t_1,t_N}$ for the ith paste from moment t_1 to moment t_N

$$X^{i'}_{t_1,t_N} = \text{Att}' X^i_{t_1,t_N} \tag{10}$$

where $X^{i'}_{t_1,t_N} = [x^{i'}_{t_1},\ldots,x^{i'}_{t_N}] \in \mathbb{R}^{N\times 1}$, $X^{i'}_{t_1,t_N}$ denotes the reconstructed temporal solder paste printing features, and the reconstructed features are constructed into a graph $G'_t = (V'_t, A)$, $V'_t = [x_t^{1'},\ldots,x_t^{M'}]$ as the input to the spatial–temporal graph convolution.

D. Spatiotemporal Graph Convolution

For solder paste printing quality anomaly prediction, the PCB of each production moment is represented by a graph, and the continuously produced PCBs constitute the spatiotemporal graph. To capture the spatial correlation and temporal closeness of the solder paste printing quality, a spatiotemporal graph convolution module is constructed. As shown in Fig. 4, each spatiotemporal graph convolution module consists of two gated CNNs, a GCN, and a batch normalization layer.

The gated CNN learns the quality variation pattern of a single solder paste in the time dimension, expressed as follows:

$$\mathcal{Y}^i_c = \big(W_{c1} * \mathcal{X}^i_c + b_{c1}\big) \bigotimes \sigma\big(W_{c2} * \mathcal{X}^i_c + b_{c2}\big) \tag{11}$$

where W_{c1} and W_{c2} are convolution kernels, b_{c1} and b_{c2} are biases, they are all trainable parameters, σ is the nonlinear activation function sigmoid, $\bigotimes$ is the product of elements between matrices, $\mathcal{X}^i_c$ denotes the input of layer i gated CNN, and $\mathcal{Y}^i_c$ denotes the output of layer i gated CNN.

The GCN mines the correlation of printing quality variation patterns among solder pastes, as shown in the following equation:

$$\begin{aligned}\mathcal{Y}^i_g &= g_\theta *_\mathcal{G} \mathcal{X}^i_g = g_\theta(L)\mathcal{X}^i_g \\ &= g_\theta\big(U\Lambda U^T\big)\mathcal{X}^i_g = U g_\theta(\Lambda)U^T\mathcal{X}^i_g\end{aligned} \tag{12}$$

where g_θ is the kernel, $*_\mathcal{G}$ is the graph convolution operation, L is the normalized Laplacian matrix $\mathcal{X}^i_g$ denotes the layer i GCN input, and $\mathcal{Y}^i_g$ is the layer i GCN output

$$L = I_M - D^{-\frac{1}{2}}AD^{-\frac{1}{2}} = U\Lambda U^T \in \mathbb{R}^{M\times M} \tag{13}$$

where U is the matrix of eigenvectors of regularized adjacency matrix L and $D_{ii} = \sum_j A_{ij}$. Due to the high operational complexity, the above equation needs to be simplified

$$\mathcal{Y}^i_g = g_\theta *_\mathcal{G} \mathcal{X}^i = g_\theta(L)\mathcal{X}^i_g \approx \sum_{k=0}^{K-1}\theta_k T_k\big(\widetilde{L}\big)\mathcal{X}^i_g \tag{14}$$

where $T_k(\widetilde{L})$ is the kth-order Chebyshev approximation of $\widetilde{L} = (2L/\lambda_{\max}) - I_M$. $\lambda_{\max}$ is the maximum eigenvalue of L. Assume further that $\lambda_{\max} \approx 2$

$$\begin{aligned}\mathcal{Y}^i_g &\approx \theta_0\mathcal{X}^i_g + \theta_1(L - I_M)\mathcal{X}^i_g \\ &\approx \theta_0\mathcal{X}^i_g - \theta_1\Big(D^{-\frac{1}{2}}AD^{-\frac{1}{2}}\Big)\mathcal{X}^i_g.\end{aligned} \tag{15}$$

Let $\theta_0 = -\theta_1$, then

$$\mathcal{Y}^i_g \approx \theta_0\Big(I_M + D^{-\frac{1}{2}}AD^{-\frac{1}{2}}\Big)\mathcal{X}^i_g \approx \theta_0\widetilde{D}^{-\frac{1}{2}}\widetilde{A}\widetilde{D}^{-\frac{1}{2}}\mathcal{X}^i_g \tag{16}$$

where $\widetilde{A} = A + I_M$ and $\widetilde{D}_{ii} = \sum_j \widetilde{A}_{ij}$.

E. Loss Function

Let the output of the last layer of the gated CNN be $\mathcal{Y}^5_c$, and the final output is obtained after the fully connected layer

$$\widetilde{\mathcal{G}} = \sigma_o\big(W_f\mathcal{Y}^5_c + b_f\big). \tag{17}$$

Our goal is to perceive the anomaly in advance by accurately predicting the solder paste printing quality. Considering that the abnormal samples of solder paste printing quality are much less than normal samples, the weight of abnormal samples must be increased to prevent spurious low error indicators, and here the weighted average absolute error $\mathcal{L}_{\text{WMAE}}$ is designed

$$\mathcal{L}_{\text{WMAE}} = \frac{1}{TM}\sum_t\sum_i \omega_N\big(1 - C^t_i\big)\big|y^t_i - \widetilde{y}^t_i\big| + \omega_P C^t_i\big|y^t_i - \widetilde{y}^t_i\big| \tag{18}$$

where C^t_i is the ith solder paste quality category label at moment t, abnormal label is 1 and normal label is 0, y^t_i is the ith solder paste quality at moment t, $\widetilde{y}^t_i$ is the corresponding predicted value, ω_P is the category weight of the abnormal sample, and ω_N is the category weight of the normal sample.

The total loss function is as follows:

$$\mathcal{L} = \mathcal{L}_{\text{WMAE}} + \mu\|\theta\|_2 \tag{19}$$

where θ is the model parameters and μ is the hyperparameter.

IV. Experimental Results and Analysis

A. Experimental Settings

1) Dataset Description: Following the solder paste printing process, there is a potential for misalignment in both the X- and Y-directions relative to the PCB pads. In addition, the deposited volume may deviate from the specified standard. Consequently, it is crucial to inspect the printing results. We collected six days of solder paste printing inspection data from the production line and obtained 11 365 available inspection records after data cleaning. Each PCB contains 3152 pad inspection results, and each inspection result contains solder paste volume, solder paste offset in the X-direction,

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TABLE I
EXPERIMENTAL HYPERPARAMETERS

Solder Paste Printing Quality	$T=5$		$T=1$	
	ω_P	λ	ω_P	λ
X-Direction Position Offset	250	0.3	500	0.3
Y-Direction Position Offset	225	0.2	225	0.2
Volume	40	0.4	20	0.4

solder paste offset in Y-direction, and other inspection contents. We select three typical abnormalities for detection: insufficient solder paste, X-direction position offset defect, and Y-direction position offset defect. PCBs with insufficient solder paste accounted for 18.79% of the total samples, PCBs with Y-direction offset defects accounted for 1.29%, and PCBs with X-direction offset defects accounted for 0.25%. To reduce the oscillation of the network, we convert the raw data in percentage form to decimals. A sliding window is used to process the data, setting the window size to 40, the sliding step size to 1, and the prediction window size T to 1 or 5. The 65% of the data is divided into the training set and the 35% into the test set.

2) Experimental Metrics: The $F1$ score and accuracy are chosen to measure the model performance. The $F1$ score is an overall measure of the model's miss and false alarm rates for solder paste printing defects. The $F1$ score is in the range of [0, 1]. When the $F1$ score is 1, it means that the model achieves perfect performance in predicting solder paste printing anomaly. When the $F1$ score is 0, it means that the model breaks down and completely fails to predict solder paste printing anomaly.

To calculate the $F1$ score, we introduce true positive (TP), true negative (TN), false positive (FP), and false negative (FN). Details of TP, TN, FP, and FN are shown below.

1) *TP:* The number of defective products that are accurately predicted.
2) *TN:* The number of qualifying products that are accurately predicted.
3) *FP:* The number of qualifying products that are incorrectly predicted to be defective.
4) *FN:* The number of defective products that are incorrectly predicted to be qualified.

As shown in (20), the Recall measures the miss alarm rate. The Precision measures the false alarm rate as shown in (21).

The $F1$ score is a combination of Recall and Precision

$$\text{Recall} = \frac{\text{TP}}{\text{TP}+\text{FN}} \tag{20}$$

$$\text{Precision} = \frac{\text{TP}}{\text{TP}+\text{FP}} \tag{21}$$

$$F1 = \frac{2\cdot\text{Recall}\cdot\text{Precision}}{\text{Recall}+\text{Precision}}. \tag{22}$$

3) Experimental Hyperparameters: Regularization factor μ is 0.002, and the category weight ω_N of the normal sample is 1. The batch size is 32 and the learning rate is 0.001. The training epoch is set to 80. Other hyperparameters are shown in Table I. Our method is implemented in a high-performance server with GeForce RTX 3090TI GPU.

4) Baselines: To ensure fairness and to prove the validity of our method, the following methods are chosen for comparison. Each experiment is repeated fivefold, and then the mean and standard deviation are calculated.

1) *IAP [22]:* Manual design features with adaptive boosting technology to predict defective solder paste printing.
2) *DTCWT-LSTM [26]:* The original solder paste printing quality data is filtered and reconstructed using the dual-tree complex wavelet transform, and then manual features are devised as input to the LSTM for prediction.
3) *GRU-Single [30]:* Quality prediction is performed by entering solder paste printing quality data for a single pad at a time into the GRU. The predicted results are then compared with the detection threshold for anomaly detection.
4) *GRU-Global [30]:* Based on the overall historical data of solder paste printing quality, the GRU is utilized to simultaneously predict the solder paste printing quality of the entire PCB. The predicted results are then checked against the detection standard for anomaly detection.
5) *LSTM-Single [31]:* Quality anomaly prediction using LSTM by inputting solder paste printing quality data for a single pad at a time. The predicted results are then compared with the detection threshold for anomaly detection.
6) *LSTM-Global [31]:* Simultaneously predict the entire PCB solder paste printing quality based on the overall historical solder paste printing quality data utilizing LSTM. The predicted results are then checked against the detection standard for anomaly detection.
7) *2-DConvLSTMAE [32]:* The quality prediction is performed by using ConvLSTM to learn the temporal closeness of time series and the spatial relationship of gridding, and then the prediction results are compared with the detection standards for anomaly detection.
8) *MRFGCN [33]:* A multireceptor field graph convolutional network for anomaly diagnosis uses multiple receptive fields to learn anomalous features and fuses the learned features for feature enhancement. We use the three receptive fields recommended in this article.
9) *SegRNN [34]:* For long-time prediction, a segmented RNN network employs a strategy of segmented iteration and parallel multistep prediction, thereby improving prediction accuracy and inference speed.
10) *FCSTGNN [35]:* For temporal prediction, a fully connected spatiotemporal graph neural network uses fully connected graph convolution with a moving pool GNN layer to efficiently capture spatiotemporal dependencies to learn efficient representations.

B. Experimental Results

1) Comparison With Baseline Methods: Table II shows the experimental results of the baselines and our method in predicting solder paste insufficiency, X-direction position offset defects, and Y-direction position offset defects at different periods. IAP, DTCWT-LSTM, GRU-Single, GRU-Gloabl, LSTM-Single, LSTM-Gloabl, 2-DConvLSTMAE, MRFGCN, SegRNN, FCSTGNN as well as our method, the average $F1$ scores for the three typical types of defects under two

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TABLE II
EXPERIMENTAL RESULTS OF DIFFERENT METHODS ON THREE SOLDER PASTE ANOMALIES

Metrics	Method	Defective X-Direction Position Offset		Defective Y-Direction Position Offset		Insufficient Solder Paste	
		$T=1$	$T=5$	$T=1$	$T=5$	$T=1$	$T=5$
		Mean/Std	Mean/Std	Mean/Std	Mean/Std	Mean/Std	Mean/Std
Accuracy	IAP	0.980/0.000	0.981/0.000	0.893/0.000	0.560/0.000	0.690/0.000	0.400/0.000
	DTCWT-LSTM	0.002/0.000	0.010/0.000	0.004/0.000	0.020/0.000	0.083/0.000	0.236/0.000
	GRU-Single	0.957/0.018	0.929/0.028	0.979/0.011	0.729/0.040	0.783/0.013	0.686/0.014
	GRU-Global	0.976/0.003	0.981/0.001	0.969/0.001	0.785/0.015	0.081/0.000	0.236/0.000
	LSTM-Single	0.964/0.011	0.958/0.025	0.979/0.011	0.729/0.040	0.866/0.029	0.691/0.011
	LSTM-Global	0.986/0.001	0.984/0.001	0.682/0.351	**0.941/0.044**	0.081/0.000	0.236/0.000
	2-DConvLSTMAE	**0.998/0.000**	**0.988/0.003**	0.004/0.000	0.020/0.000	0.081/0.000	0.236/0.000
	MRFGCN	0.979/0.003	0.969/0.025	0.981/0.002	0.859/0.050	0.925/0.005	0.681/0.018
	SegRNN	0.981/0.000	0.973/0.000	0.985/0.000	0.829/0.000	0.081/0.000	0.236/0.000
	FCSTGNN	0.974/0.000	0.980/0.000	0.553/0.065	0.166/0.000	0.081/0.000	0.236/0.000
	Our Method	0.983/0.003	0.986/0.002	**0.988/0.006**	0.894/0.168	**0.932/0.003**	**0.744/0.037**
F1	IAP	0.149/0.000	0.460/0.000	0.005/0.000	0.055/0.000	0.211/0.000	0.417/0.000
	DTCWT-LSTM	0.005/0.000	0.020/0.000	0.008/0.000	0.040/0.000	0.150/0.000	0.382/0.000
	GRU-Single	0.083/0.019	0.221/0.054	0.045/0.025	0.082/0.001	0.352/0.015	0.511/0.008
	GRU-Global	0.155/0.002	0.513/0.002	0.021/0.018	0.088/0.019	0.150/0.000	0.382/0.000
	LSTM-Single	0.086/0.004	0.290/0.058	0.039/0.003	0.083/0.002	0.403/0.028	0.506/0.006
	LSTM-Global	0.159/0.005	0.513/0.006	0.046/0.049	0.070/0.039	0.150/0.000	0.382/0.000
	2-DConvLSTMAE	0.000/0.000	0.102/0.204	0.008/0.000	0.040/0.000	0.150/0.000	0.382/0.000
	MRFGCN	0.138/0.016	0.305/0.053	0.046/0.008	0.094/0.003	0.481/0.016	0.461/0.002
	SegRNN	0.141/0.000	0.429/0.000	0.033/0.000	0.085/0.000	0.150/0.000	0.382/0.000
	FCSTGNN	0.153/0.000	0.500/0.000	0.012/0.003	0.038/0.000	0.150/0.000	0.382/0.000
	Our Method	**0.166/0.006**	**0.521/0.009**	**0.055/0.030**	**0.098/0.015**	**0.493/0.009**	**0.532/0.019**

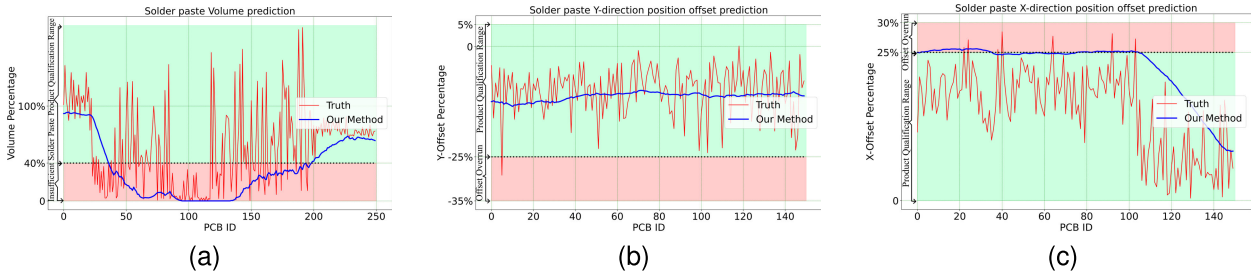

Fig. 5. Time-series prediction of solder paste printing quality for a single pad. (a) Solder paste volume prediction curve. (b) Solder paste Y-direction position offset prediction curve. (c) Solder paste X-direction position offset prediction curve.

different time scales are 0.216, 0.101, 0.215, 0.218 0.235, 0.220, 0.114, 0.254, 0.203, 0.206, and 0.311. Our approach improves $F1$ score by at least 0.057. Also, our method achieves the best $F1$ score in all six scenarios. The average Accuracy of the above methods in different scenarios is 0.751, 0.059, 0.843, 0.671, 0.865, 0.712, 0.375, 0.899, 0.680, 0.498, and 0.921, respectively. Our approach improves Accuracy by at least 0.022. This demonstrates the important role of solder paste printing quality variation spatial correlation in the prediction of solder paste printing abnormality. It can also be found that MRFGCN with a graph structure achieves the second-best performance among all methods to our method. This proves that modeling the PCB layout as a graph helps to improve the prediction of defects.

It can be discovered that our method is significantly better than the baseline methods in predicting the defective production effectively in terms of X-direction position offset defects and solder paste insufficiency, while all methods perform poorly on Y-direction position offset defects. The reasons for these are shown in Fig. 5. The predictions of solder paste volume, Y-direction offset, and X-direction offset during solder paste printing are shown sequentially in Fig. 5. The red regions in Fig. 5 indicate defects exceeding the set threshold values. After data desensitization, the threshold for solder paste insufficiency is 40%. The qualifying interval for X-direction and Y-direction offsets is $[-25\%, 25\%]$. As can be seen from the time-series curves of solder paste offsets in the Y-direction, these offset defects are mainly caused by severe jitter. Therefore, it is difficult to track the deterioration trend, resulting in poor model performance. Observing the time curves of solder paste volume and X-direction offset, significant trend changes are apparent during defect occurrences. Thus, our approach achieves effective predictive outcomes. Furthermore, the X-direction offset values are larger in the early stage, so the predicted values are also slightly larger to accurately predict the offset defects. When the X-direction offset value decreases at a later stage, the predicted value follows immediately. This demonstrates the ability of our method to capture the trend of quality change.

2) Estimated Extent of Anomaly: To provide engineers with information on the extent of solder paste printing anomaly, we classify the extent of solder paste printing anomaly into levels. As shown in Fig. 6, taking solder paste printing insufficiency as an example, we classify three levels, qualified, slight insufficiency, and severe insufficiency. The qualified product is solder paste volume greater than 40%, the interval for slight insufficiency is $[20\%, 40\%]$, and severe insufficiency is $[0, 20\%]$. In Fig. 6, it can be seen that there are

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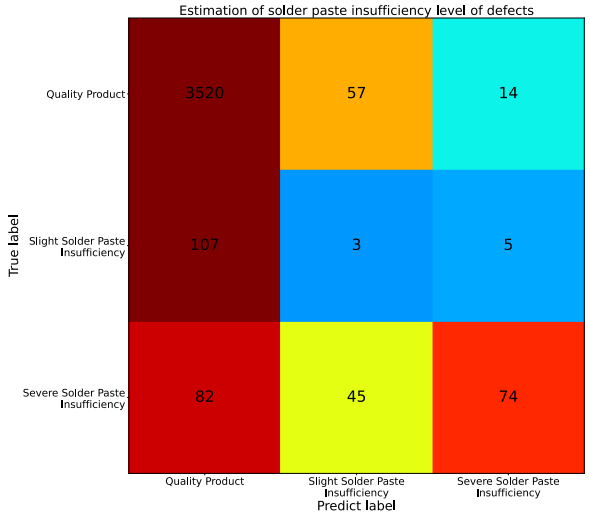

Fig. 6. Predictive effect of different levels of anomalies for the solder paste volume.

3520 good products, three slight solder paste insufficiencies, and 74 severe solder paste insufficiencies that are correctly predicted. Our model achieves better prediction results for the level of defective products. But at the same time, it can also be seen that there are 107 slight insufficiencies and 82 severe insufficiencies that are incorrectly predicted as good products. The reason for the prediction error of solder paste slight insufficiency may be that slight out-of-qualification ranges can make it difficult for the model to predict accurately. For severe insufficiency, it can be seen from Fig. 5(a) that there exists a lot of solder paste volume abrupt change to 0. For the factory, it is important that we already successfully predict the trend of deteriorating quality and thus adjust the parameters to reduce defective products.

3) Approaches Complexity Analysis: We compare the computational cost of our method with other baseline methods on the same GPU server, where all library versions are kept constant. In Table III, the training time is the time to train one epoch on the training set on a single GPU when the prediction window $T = 1$. The testing time refers to the inference time for the entire test set of about 4000 samples. Our model has the seventh-highest training time out of ten models and the eighth-highest testing time. This is because to achieve higher performance, the model becomes more complex, thus slightly sacrificing training time and testing time. In practical applications, the training time reflects the time cost required to build the model. For four days of production data, our model spent 71 s per epoch and trained a total of 80 epochs, which is about 1.5 h. A ratio of 96/1.5 between production data time and training time is acceptable. In practice, the test time reflects the real-time performance of the model. Each time a PCB is printed, the model makes an inference prediction. Therefore, the model's single inference time needs to be smaller than the PCB printing interval to meet the practical requirements. For a single test sample, it takes only about 0.005 s for our model to give a prediction result. According to our research in the factory, the interval of solder paste printing is about 15 s. Thus, the real-time performance can fully meet the demand. The model parameters reflect the storage costs incurred in model construction, and our model is positioned in the middle tier. Our model can still fit within the memory of a single GPU, without causing excessive hardware costs.

TABLE III
MODEL COMPLEXITY

Models	Parameters Number	Training Time(s)	Testing Time(s)
DTCWT-LSTM	96	1	1
GRU-Single	32465	11	1
GRU-Global	59633737	8	1
LSTM-Single	32553	9	1
LSTM-Global	7450272	11	1
2-DConvLSTMAE	397504329	394	47
MRFGCN	13153	3	1
SegRNN	2388747	88	17
FCSTGNN	7013	110	34
Our Method	79081	71	20

4) Ablation Experiments: To analyze the role played by the different components of our method in anomaly prediction, we designed three different variants by removing some of the components and observing the prediction performance of the remaining parts.

1) *Variant-NTA:* To verify the effect of production time interval on solder paste printing quality, we remove the attention based on production time and the rest is consistent with our method.
2) *Variant-NGCN:* To verify the effect of modeling the PCB layout as a graph on the quality of solder paste printing, we remove the GCN module and the rest is consistent with our approach.
3) *Variant-NGatedCNN:* To verify the effect of the temporal module on the prediction of solder paste printing quality, we remove the gated CNN module and keep the rest in line with our approach.

The results are shown in Table IV. It shows that the introduction of attention based on production time significantly improves the prediction of defective products, especially in the defective X-direction position offset, where Variant-NTA's $F1$ score is 0.412 when the prediction window $T = 5$, while our design of production time-based attention improves the $F1$ score to 0.521. The standard deviation of the predictive metrics is also generally reduced, which improves the stability of the model. This suggests that production time-based concerns capture the effect of production time on the quality of solder paste printing, specifically referring to the gradual change in the physicochemical properties of the paste, such as viscosity, over time. The average Accuracy of Variant-NGCN is 0.725 and the average $F1$ score is 0.243, which shows a significant decrease compared to our method's average Accuracy of 0.921 and average $F1$ score of 0.311. This proves the necessity of modeling the graph structure based on the PCB layout, which can effectively improve the prediction. The average Accuracy of Variant-NGatedCNN is 0.791 and the average $F1$ score is 0.234. Since we use real time-series production data for PCB solder paste printing defects prediction, the temporal module is responsible for extracting the temporal evolution pattern in the production

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TABLE IV
ABLATION EXPERIMENTAL RESULTS

Metrics	Method	Defective X-Direction Position Offset		Defective Y-Direction Position Offset		Insufficient Solder Paste	
		$T=1$	$T=5$	$T=1$	$T=5$	$T=1$	$T=5$
		Mean/Std	Mean/Std	Mean/Std	Mean/Std	Mean/Std	Mean/Std
Accuracy	Variant-NTA	0.978/0.009	0.985/0.002	0.201/0.395	0.415/0.457	0.932/0.004	0.677/0.103
	Variant-NGCN	0.978/0.009	0.979/0.001	0.803/0.127	0.490/0.397	0.760/0.021	0.429/0.035
	Variant-NGatedCNN	0.974/0.000	0.981/0.001	**0.992/0.000**	**0.979/0.002**	0.587/0.000	0.236/0.000
	Our Method	**0.983/0.003**	**0.986/0.002**	0.988/0.006	0.894/0.168	**0.932/0.003**	**0.744/0.037**
F1	Variant-NTA	0.152/0.008	0.412/0.206	0.018/0.019	0.071/0.026	0.470/0.022	0.499/0.032
	Variant-NGCN	0.150/0.003	0.492/0.011	0.024/0.006	0.068/0.027	0.302/0.012	0.426/0.009
	Variant-NGatedCNN	0.152/0.001	0.511/0.001	**0.061/0.000**	0.057/0.020	0.242/0.000	0.382/0.000
	Our Method	**0.166/0.006**	**0.521/0.009**	0.055/0.030	**0.098/0.015**	**0.493/0.009**	**0.532/0.019**

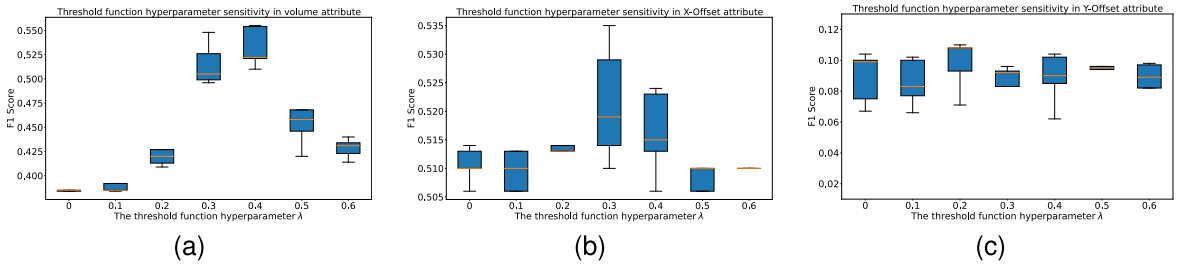

Fig. 7. Solder paste printing anomaly prediction correlation threshold sensitivity analysis. Fixed abnormal sample weights ω_P and adjusted correlation threshold. (a) Correlation threshold sensitivity in volume attribute. (b) Correlation threshold sensitivity in X-Offset attribute. (c) Correlation threshold sensitivity in Y-Offset attribute.

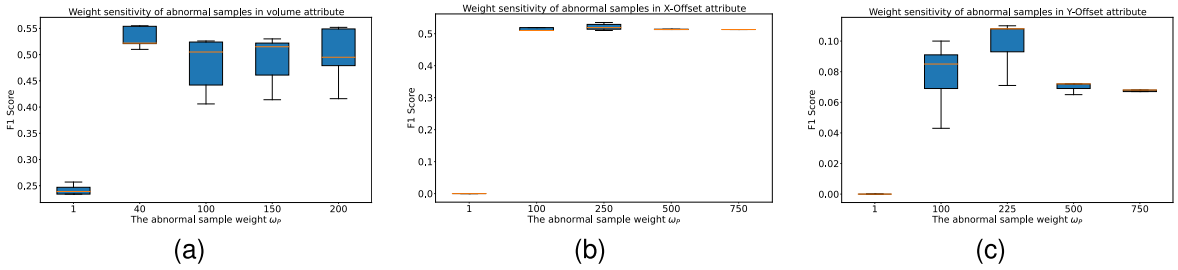

Fig. 8. Solder paste printing anomaly prediction abnormal sample weight sensitivity analysis. Fixed correlation threshold λ and adjusted abnormal sample weight. (a) Weight sensitivity in volume attribute. (b) Weight sensitivity in X-Offset attribute. (c) Weight sensitivity in Y-Offset attribute.

data, which has an important impact on the prediction results.

5) Hyperparameters Analysis: Fig. 7 illustrates the effect of the solder paste printing quality correlation threshold on the anomaly prediction ability of the model when $T = 5$. We fix the weights of the abnormal samples, adjust the correlation threshold, and repeat the experiment five times. In Fig. 7, the green triangle represents the mean of the $F1$ scores and the orange line represents the median. The prediction of solder paste insufficiency is significantly more sensitive to the correlation threshold compared to the prediction of X-direction position offset defects and Y-direction position offset defects. This is because the X-direction position offset has a higher global correlation due to the PCB along the X-direction into the solder paste printer. The Y-direction position offset defects exhibit abrupt characteristics. Existing methods perform poorly in detecting these defects, resulting in the correlation threshold having minimal impact on the experimental results.

Fig. 8 shows the effect of the abnormal sample weight on the experimental results when $T = 5$. We fix the correlation threshold, adjust the abnormal sample weight ω_P, and repeat each experiment five times. Compared to the correlation threshold, the model is insensitive to abnormal sample weight ω_P within a certain range. In the anomaly prediction of solder paste insufficiency, the anomaly sample weight ω_P has a stable good performance in the interval $[40, 200]$. In the X-direction position offset defect prediction, anomaly sample weight in $[100, 750]$ can achieve a better prediction. Better prediction can be achieved in the Y-direction position offset defect prediction with anomaly sample weight ω_P in the interval $[100, 225]$ as well. The abnormal sample weight is usually related to the percentage of abnormal samples in the total sample, the higher the percentage, the lower the abnormal sample weight, for example, the abnormal sample weight of insufficient solder paste is significantly lower than the abnormal sample weights of X-direction position offset defects and Y-direction position offset defects, and the frequency of insufficient solder paste is also much higher than them.

V. CONCLUSION

In this article, we propose a PCB layout-based spatiotemporal graph convolution network for solder paste printing anomaly prediction. Compared with other methods, our method fully considers the spatial correlation of the variation of solder paste printing quality and can effectively predict the

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defective products in the solder paste printing process, thus helping engineers to reduce the defective products and improve production efficiency.

Since many reasons can cause solder paste printing quality abnormality, in the future, we will analyze potential causes of printing anomaly, such as warpage/shrinkage, based on predicted printing quality anomaly as well as available conditions including the state of the solder paste printing machine and process parameters. Furthermore, in response to the identified anomaly causes, the solder paste printing machine parameters are dynamically adjusted to eliminate defective products during the solder paste printing process.

REFERENCES

[1] D. J. Zhou and X. Y. Chen, "Discussion on application of intelligent manufacturing technology in SMT product assembly manufacturing system," *MATEC Web Conf.*, vol. 63, p. 02035, 2016.

[2] R. Ding, L. Dai, G. Li, and H. Liu, "TDD-Net: A tiny defect detection network for printed circuit boards," *CAAI Trans. Intell. Technol.*, vol. 4, no. 2, pp. 110–116, 2019.

[3] S. Venkateswaran, K. Srihari, J. H. Adriance, and G. R. Westby, "A realtime process control system for solder paste stencil printing," in *Proc. 21st IEEE/CPMT Int. Electron. Manuf. Technol. Symp. (IEMT Symp.)*, Oct. 1997, pp. 62–67.

[4] S. Alelaumi, N. Khader, J. He, S. Lam, and S. W. Yoon, "Residue buildup predictive modeling for stencil cleaning profile decision-making using recurrent neural network," *Robot. Comput.-Integr. Manuf.*, vol. 68, Apr. 2021, Art. no. 102041.

[5] S. Alelaumi, J. He, Y. Li, N. Khader, and S. W. Yoon, "Cleaning profile classification using convolutional neural network in stencil printing," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 11, no. 11, pp. 2003–2011, Nov. 2021.

[6] A. Geczy, M. Fejos, and L. Tersztyánszky, "Investigating and compensating printed circuit board shrinkage induced failures during reflow soldering," *Soldering Surf. Mount Technol.*, vol. 27, no. 2, pp. 61–68, Apr. 2015.

[7] P. Martinek, B. Illés, N. Codreanu, and O. Krammer, "Investigating machine learning techniques for predicting the process characteristics of stencil printing," *Materials*, vol. 15, no. 14, p. 4734, Jul. 2022.

[8] T. Yang, T.-N. Tsai, and J. Yeh, "A neural network-based prediction model for fine pitch stencil-printing quality in surface mount assembly," *Eng. Appl. Artif. Intell.*, vol. 18, no. 3, pp. 335–341, Apr. 2005.

[9] D. C. Montgomery, J. Bert Keats, L. A. Perry, J. R. Thompson, and W. S. Messina, "Using statistically designed experiments for process development and improvement: An application in electronics manufacturing," *Robot. Comput.-Integr. Manuf.*, vol. 16, no. 1, pp. 55–63, Feb. 2000.

[10] Y.-H. Yoo, U.-H. Kim, and J.-H. Kim, "Convolutional recurrent reconstructive network for spatiotemporal anomaly detection in solder paste inspection," *IEEE Trans. Cybern.*, vol. 52, no. 6, pp. 4688–4700, Jun. 2022.

[11] N. Khader and S. W. Yoon, "Online control of stencil printing parameters using reinforcement learning approach," *Proc. Manuf.*, vol. 17, pp. 94–101, Jan. 2018.

[12] H. Lu, J. He, D. Won, and S. W. Yoon, "A guided evolutionary search approach for real-time stencil printing optimization," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 11, no. 2, pp. 333–341, Feb. 2021.

[13] N. Khader, J. Lee, D. Lee, S. W. Yoon, and H. Yang, "Multi-objective optimization approach to enhance the stencil printing quality," in *Proc. 29th Int. Conf. Flexible Autom. Intell. Manuf. (FAIM)*, vol. 38, 2019, pp. 163–170.

[14] N. Khader and S. W. Yoon, "Adaptive optimal control of stencil printing process using reinforcement learning," *Robot. Comput.-Integr. Manuf.*, vol. 71, Oct. 2021, Art. no. 102132.

[15] B. Wang, Y. Lin, S. Guo, and H. Wan, "GSNet: Learning spatial–temporal correlations from geographical and semantic aspects for traffic accident risk forecasting," in *Proc. AAAI Conf. Artif. Intell.*, vol. 35, pp. 4402–4409, 2021.

[16] L. Xia et al., "Spatial–temporal sequential hypergraph network for crime prediction with dynamic multiplex relation learning," in *Proc. IJCAI*, Aug. 2021, pp. 1631–1637.

[17] X.-X. Yin, Y. Miao, and Y. Zhang, "Time series based data explorer and stream analysis for anomaly prediction," *Wireless Commun. Mobile Comput.*, vol. 2022, Apr. 2022, Art. no. 5885904.

[18] T.-N. Tsai and L.-H. Chen, "Monitoring of the stencil printing process using a modified regression residual control chart: An empirical study," *Int. J. Ind. Eng., Theory, Appl. Pract.*, vol. 16, no. 4, pp. 248–259, 2009.

[19] N. Khader and S. W. Yoon, "Stencil printing process optimization to control solder paste volume transfer efficiency," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 8, no. 9, pp. 1686–1694, Sep. 2018.

[20] T.-N. Tsai, "Improving the fine-pitch stencil printing capability using the Taguchi method and Taguchi fuzzy-based model," *Robot. Comput.-Integr. Manuf.*, vol. 27, no. 4, pp. 808–817, Aug. 2011.

[21] O. Krammer, T. Al-Ma'aiteh, P. Martinek, K. Anda, and N. Balogh, "Predicting the transfer efficiency of stencil printing by machine learning technique," in *Proc. 43rd Int. Spring Seminar Electron. Technol. (ISSE)*, May 2020, pp. 1–6.

[22] S. Alelaumi, H. Wang, H. Lu, and S. W. Yoon, "A predictive abnormality detection model using ensemble learning in stencil printing process," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 10, no. 9, pp. 1560–1568, Sep. 2020.

[23] W. Wang, W. Gui, and Z. Xu, "Solder paste printing quality prediction model based on PSO optimization," in *Methods and Applications for Modeling and Simulation of Complex Systems*. Singapore: Springer, 2022, pp. 538–547.

[24] N. Thielen et al., "Machine learning based quality prediction for solder paste dispensing in electronics production," in *Proc. IEEE 24th Electron. Packag. Technol. Conf. (EPTC)*, Dec. 2022, pp. 858–863.

[25] R. Seidel, B. Rachinger, N. Thielen, K. Schmidt, S. Meier, and J. Franke, "Development and validation of a digital twin framework for SMT manufacturing," *Comput. Ind.*, vol. 145, Feb. 2023, Art. no. 103831.

[26] H. Wang, H. Lu, S. M. Alelaumi, and S. W. Yoon, "A wavelet-based multi-dimensional temporal recurrent neural network for stencil printing performance prediction," *Robot. Comput.-Integr. Manuf.*, vol. 71, Oct. 2021, Art. no. 102129.

[27] O. Krammer, B. Gyarmati, A. Szilágyi, B. Illés, D. Bušek, and K. Dušek, "The effect of solder paste particle size on the thixotropic behaviour during stencil printing," *J. Mater. Process. Technol.*, vol. 262, pp. 571–576, Dec. 2018.

[28] O. Krammer et al., "Investigating the thixotropic behaviour of type 4 solder paste during stencil printing," *Soldering Surf. Mount Technol.*, vol. 29, no. 1, pp. 10–14, Feb. 2017.

[29] C.-Y. Huang, "Applying the Taguchi parametric design to optimize the solder paste printing process and the quality loss function to define the specifications," *Soldering Surf. Mount Technol.*, vol. 30, no. 4, pp. 217–226, Sep. 2018.

[30] K. Cho et al., "Learning phrase representations using RNN encoder–decoder for statistical machine translation," in *Proc. Conf. Empirical Methods Natural Language Process. (EMNLP)*, 2014, pp. 1724–1734.

[31] S. Hochreiter and J. Schmidhuber, "Long short-term memory," *Neural Comput.*, vol. 9, no. 8, pp. 1735–1780, 1997.

[32] A. Essien and C. Giannetti, "A deep learning model for smart manufacturing using convolutional LSTM neural network autoencoders," *IEEE Trans. Ind. Informat.*, vol. 16, no. 9, pp. 6069–6078, Sep. 2020.

[33] T. Li, Z. Zhao, C. Sun, R. Yan, and X. Chen, "Multireceptive field graph convolutional networks for machine fault diagnosis," *IEEE Trans. Ind. Electron.*, vol. 68, no. 12, pp. 12739–12749, Dec. 2021.

[34] S. Lin, W. Lin, W. Wu, F. Zhao, R. Mo, and H. Zhang, "SegRNN: Segment recurrent neural network for long-term time series forecasting," 2023, *arXiv:2308.11200*.

[35] Y. Wang et al., "Fully-connected spatial–temporal graph for multivariate time-series data," in *Proc. AAAI Conf. Artif. Intell.*, 2024, vol. 38, no. 14, pp. 15715–15724.

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